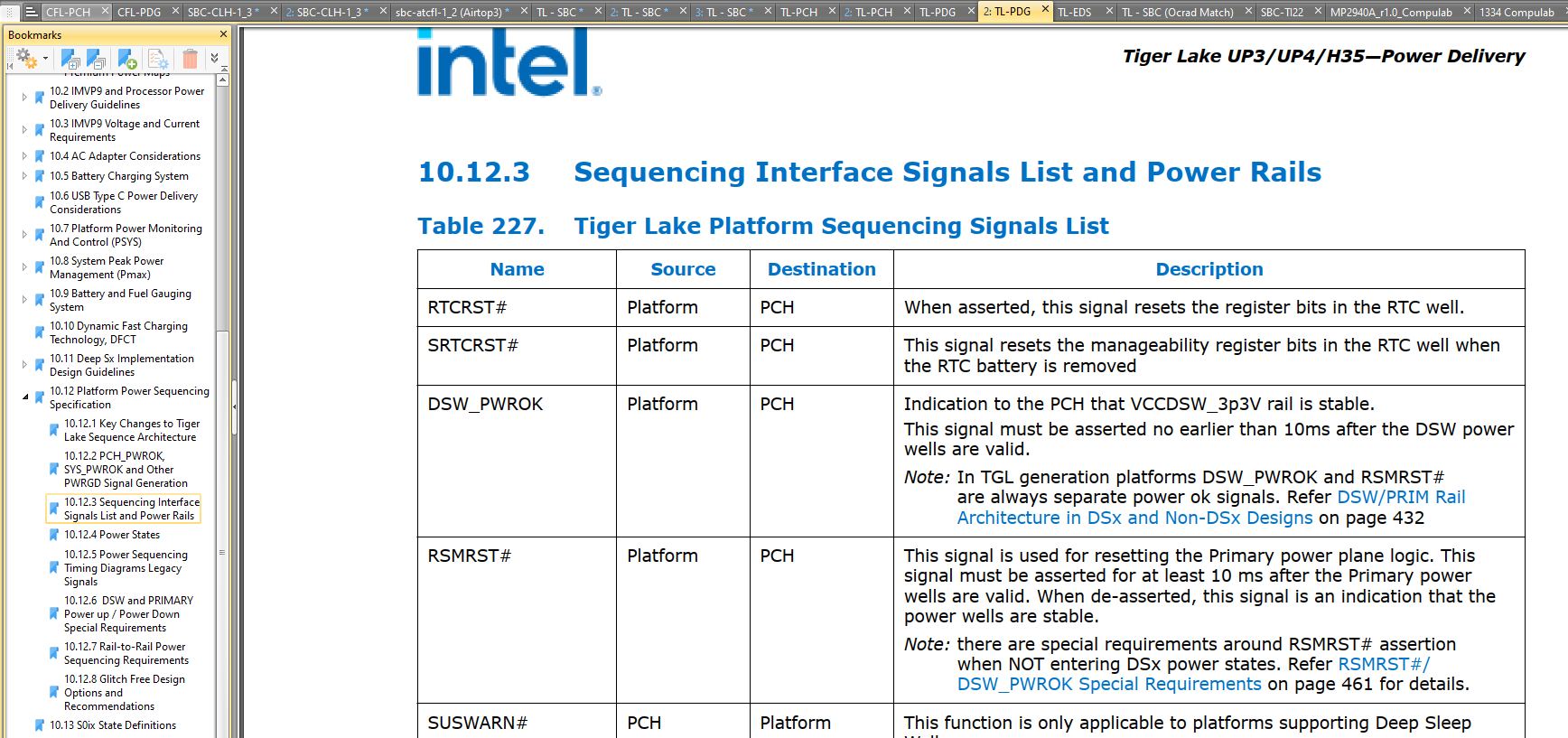
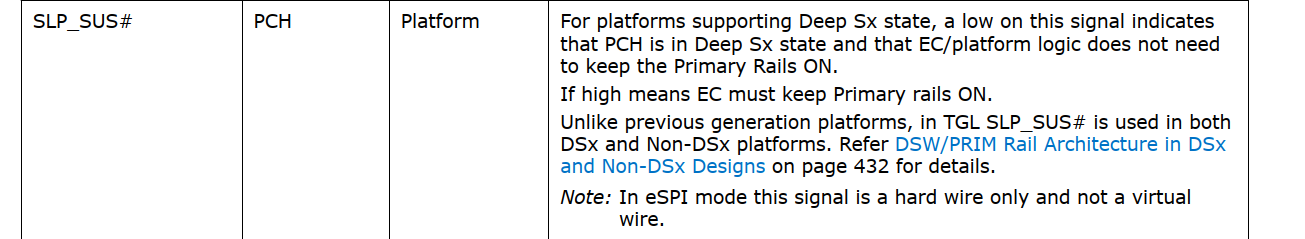
**PDG:**

**Sequencing Interface Signals List and Power Rails**



SLP\_SUS#:

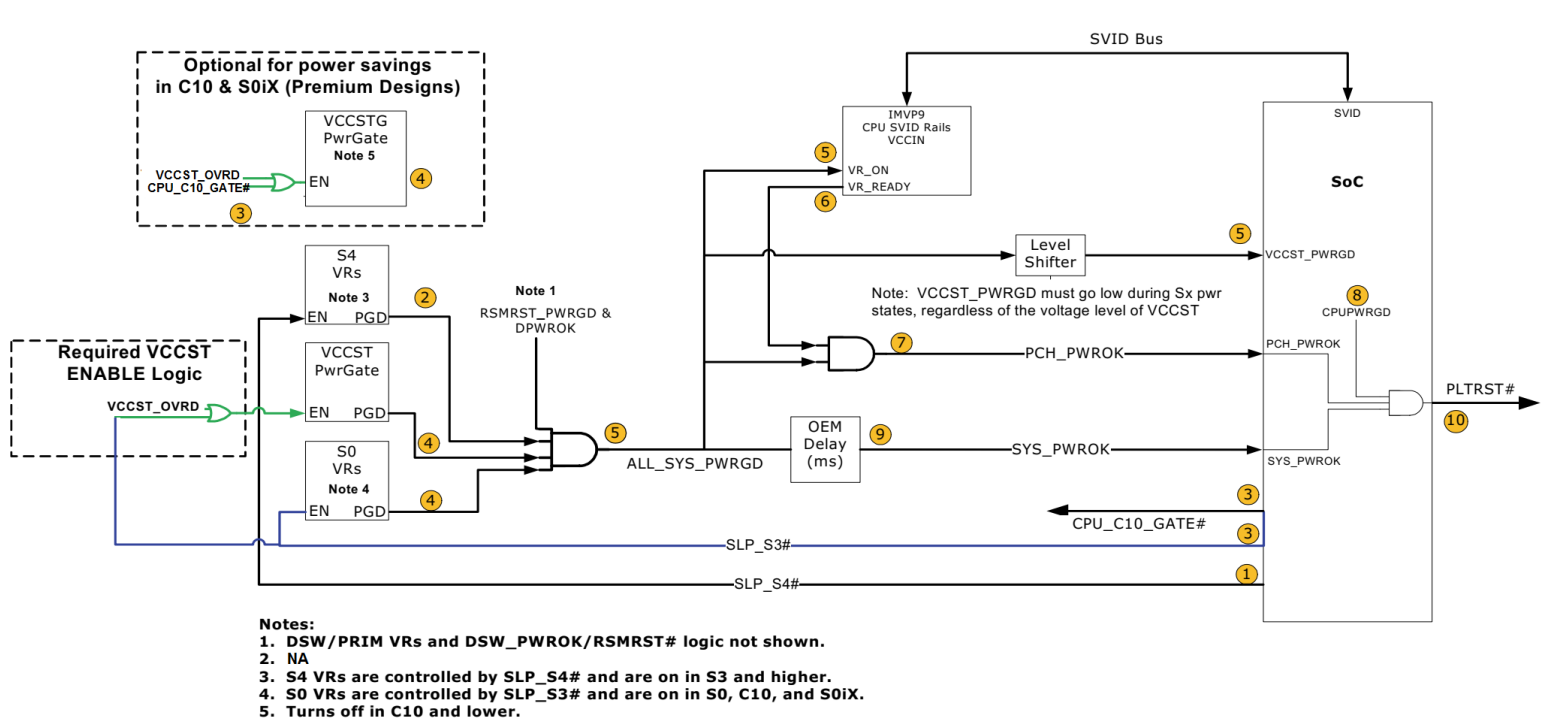


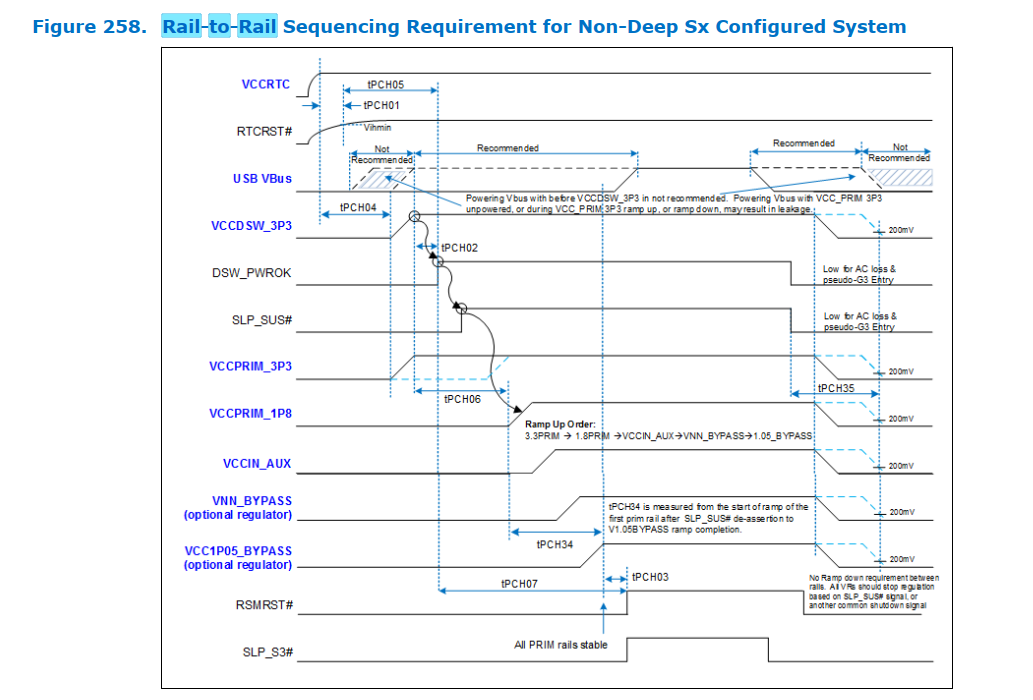
If SLP\_SUS#=0 🡪

**Power Up:**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **SL. No** |  | **Rail Name** |  | **Net Name in SCH [Fill up by customer own design]** |  |
| 1 |  | VCCRTC | 1 | +VCCPRTC\_3P3 | 2.0-3.3V +5% supplies for PCH RTC Well. This power is not  expected to be shut off in any of the sleep states unless the RTC battery is removed or completely drained. |
| 2 | RTCRST# | RTC\_RST\_N | When asserted, this signal resets the register bits in the RTC well. |
| 3 | SRTCRST# | SRTC\_RST\_N | This signal resets the manageability register bits in the RTC well when the RTC battery is removed |
| 4 | 2 | VCCDSW\_3P3 |  | **+VCCPDSW\_3P3** | 3.3-V supply for Deep Sx wells. If Deep Sx is not supported on the platform, tie to **VCCPRIM\_3P3.** |
| 5 | DSW\_PWROK | DSW\_PWROK | **Deep Sx Well PWROK**: Power OK Indication for the **+VCCPDSW\_3P3** voltage rail. Note: This signal is in the RTC well. This signal cannot tie with RSMRST#.  Connected to FPGA |
| 6 | SLP\_SUS# | PM\_SLP\_SUS\_N | Or platforms supporting Deep Sx state, a low on this signal **(SLP\_SUS# =0**) indicates that PCH is in Deep Sx state and that EC/platform logic does not need to keep the Primary Rails ON. (+VCCPRIM\_3P3 && VCCPRIM\_1P8) should go down.  If  **SLP\_SUS# =0 🡪 +VCCPRIM\_3P3 = 0** && **VCCPRIM\_1P8 = 0**  **If high (SLP\_SUS# =1**) **means EC must keep Primary rails ON.**  Unlike previous generation platforms, in TGL SLP\_SUS# is used in both DSx and Non-DSx platforms. Refer DSW/PRIM Rail Architecture in DSx and Non-DSx Designs on page 432 for details.  Note: In eSPI mode this signal is a hard wire only and not a virtual wire.  **SLP\_SUS# =1 indicates that** (+VCCPRIM\_3P3 && VCCPRIM\_1P8) should be ENABLED.  In TL-SBC: 226/270  In TL-SBC: 234/270 **SLP\_SUS# =1**  Enables +V3.3A and +5VA  In TL-SBC: 226/270 **SLP\_SUS# =1**  Enables +V1.8A  In TensorI20 FPGA Code: SLP\_SUS# wasn’t used to enable V33A\_ENn, but VCC was used instead (which is high when +3V3DSW is high) |
| 7 | V5.0A | 3 | +V5A |  |
| 8 |  | VCCPRIM\_3P3 | +VCCPRIM\_3P3 | PCH I/O and Misc rails 3.3V (Primary Well) |
| 9 | VCCPRIM\_1P8 | +VCCPRIM\_1P8 | PCH I/O and Misc rails 1.8V (Primary Well) |
| 10 | 4 | VCCIN\_AUX | +VCCIN\_AUX | PCH FIVR input power supply |
| ~~11~~ | ~~VNN\_BYPASS~~ |  | ~~+VCC\_VNNEXT\_1P05V~~ | **~~Optional~~** ~~BYPASS rail for PCH Prime Core Well (760mV in S0ix~~  ~~and 1.05V in Sx states) or reduced power consumption in low power states~~ |
| ~~12~~ | ~~V1.05A\_BYPASS~~ | ~~+VCC\_V1P05EXT\_1P05V~~ | **~~Optional~~** ~~BYPASS rail for PCH Primary Well (1.05V) for reduced power consumption in low power states~~ |
| 13 | RSMRST# | 5 | PM\_RSMRST\_N |  |
| 14 |  | PWRBTN# | PM\_PWRBTN\_N |  |
| 15 | 6 | SLP\_S5# | PM\_SLP\_S5\_N | This signal is for power plane control. When asserted (low), it will shutoff power to all non-critical systems in **S5 (Soft Off)** states.  Note: In eSPI mode this signal is also virtual wire on the eSPI  interface, in addition to the hard signal from PCH.Refer eSPI  Compatibility Specification (508740) and Tiger Lake Platform Controller Hub-LP External Design Specification for details. |
| 16 | SLP\_S4# |  | PM\_SLP\_S4\_N | S4 Sleep Control. This signal is for power plane control. When asserted (low), it will shut-off power to all non-critical systems in S4 (Suspend to Disk) and lower (S5).  If SLP\_S4# = 0 ,  Note: In eSPI mode this signal is also virtual wire on the eSPI  interface, in addition to the hard signal from PCH. Refer eSPI Compatibility Specification (508740) and Tiger Lake Platform Controller Hub-LP External Design Specification for details. |
| 17 | **DDR\_VPP (DDR4)** | **+V1.8U\_2.5U\_MEM {VPP}** |  |
| 18 | SLP\_S3# | 7 | PM\_SLP\_S3\_N (GOES **HIGH** ON POWER UP) | SLP\_S3# is for power plane control. This signal shuts off power to all non-critical systems when in the **S4, or S5 state.** |
| 19 |  | SLP\_S0# | PM\_SLP\_S0\_N | S0 Sleep Control: When PCH is idle and processor is in C10 state, this pin will assert to indicate VR controller can go into a light load mode. This signal can also be  connected to EC for other power management related optimizations.  If PM\_SLP\_S0\_N = 0, |
| 20 | 8 | CPU\_C10\_GATE# | CPU\_C10\_GATE\_N | Power gating control to turn off VCCSTG in C10 and lower.  Note: In eSPI mode this signal is a **hard wire** only and not a virtual wire.  External Power Gate: Control for VCCIO, VCCSTG and VCCPLL\_OC during C10. When asserted, VCCIO, VCCSTG and VCCPLL\_OC can be 0 V, however the power good indicators for these rails must remain asserted. |
| 21 | VCCST |  | +VCCST\_CPU | Sustain voltage for processor in Standby modes |
| 22 | **DDR\_VDD2 (DDR4)** | **+VDD2\_CPU** |  |
| 23 | **DDR\_VDDQ (DDR4)** | 9 | **+VDD2\_MEM (p.229/270)** |  |
| 24 |  | VCCSTG | +VCCSTG\_CPU |  |
| 25 | 10 | ALL\_SYS\_PWRGD | ALL\_SYS\_PWRGD |  |
| 26 | VCCST\_PWRGD |  | VCCST\_PWRGD | VCCST\_PWRGD is a signal on the Tiger Lake processor that indicates both the VCCST power supply and VDDQ power supply are within voltage tolerance specifications.  TL-PCH:  VccST Power Good : When asserted, an indicator to the processor this rail is now supplied by the integrated FIVR in the PCH.  During S5 to S0 and DSx to S0 transitions, the platform will need to generate the **VCCST\_PWRGD**, **PCH\_PWROK** and **SYS\_PWROK** signals to the processor. In this phase of the power up sequence, the platform and CPU S0 rails are ramped up. |
| 27 | VTT | +V\_VDD2\_VTT **{VTT}** |  |
| 28 | PCH\_PWROK (from FPGA to Processor) | 11 | PM\_PCH\_PWROK |  |
| 29 |  | VCCIN | +VCCIN | Processor FIVR input power supply |
| 30 | PROCPWRGD | CPUPWRGD |  |
| 31 | 12 | VCCIO | +VCCIO\_OUT |  |
| 32 | SYS\_PWROK |  | SYS\_PWROK |  |
| 33 | PLTRST# | PLT\_RST\_N |  |
|  |  |  |  |  |  |

**Premium PWROK (Power OK) Generation Flow Diagram**



**Rail-to-Rail Sequencing Requirement for Non-Deep Sx Configured System**:

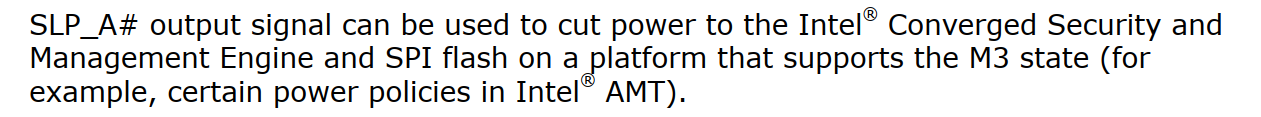
Power UP (TL-PDG p.449)

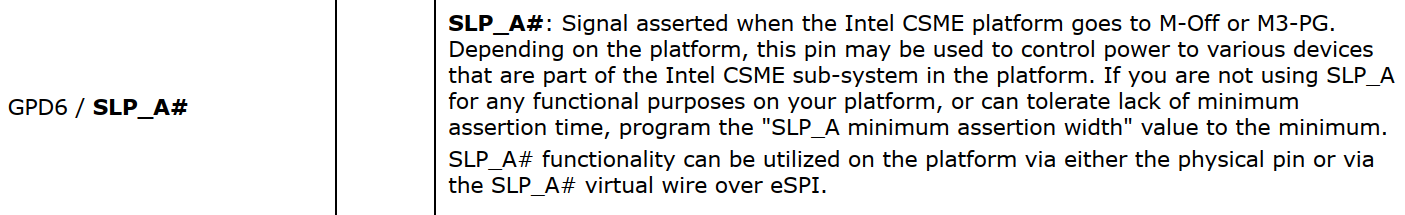
|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| **Label** | **Signal Name** | **Min** | **Max** | **Unit** | **Description** | **Controlled by** | **Chosen in FPGA** |
| **tPCH01** | VCCRTC [+VCCPRTC\_3P3] RTCRST# [RTC\_RST\_N] SRTCRST# [SRTC\_RST\_N] | 9 |  | ms | VccRTC = 2.0V to the point in time where voltage on the RTC resets equals 0.65 times the voltage present on the VccRTC rail during ramp. This measurement should be made from VccRTC = 2.0V to the first of RTCRST# or SRTCRST# reaching 0.65 \* VccRTC | PLT | done |
| **tPCH02** | From **VCCDSW\_3P3** to  **DSW\_PWROK** | 10 | 2000 | ms | VccDSW stable (@95% of full value) to DSW\_PWROK high. | PLT | 35 ms  (done in dsw\_pwrok\_block) |
| **tPCH03** | VNN\_BYPASS [+VCC\_VNNEXT\_1P05V] V1.05A\_BYPASS [+VCC\_V1P05EXT\_1P05V]  RSMRST# [PM\_RSMRST\_N] | 10 | 2000 | ms | VccPrimary stable (@95% of full value) to RSMRST# high | PLT | NA |
| **tPCH04** | VCCRTC [+VCCPRTC\_3P3] VCCDSW\_3P3 [+VCCPDSW\_3P3]  Note: how did we take care of this delay in CFL-SBC? | 9 |  | ms | VccRTC stable (@90% of full value) to start of VccDSW voltage ramp for systems with **coined RTC battery** | PCH | In Tensor I22:  In the coinless case when **3V3DSW** is up +**VCCPRTC\_3P3** is up. |
| 30 | VccRTC stable (@90% of full value) to start of VccDSW voltage ramp for systems with **coinless RTC**. Please refer to IBP#549657 for Design considerations technical advisory document without RTC battery. Earlier this timing was referred as tPCH48.(in CLH) |
| **tPCH05** | RTCRST# [RTC\_RST\_N] DSW\_PWROK | 1 |  | us | RTCRST# high (voltage above ViH\_min) to DSW\_PWROK high (when voltage crosses ViL\_max such that internally it might be resolved as a logic ‘1’) | PLT |  |
|  |
|  |
|  |
| **tPCH06** | VCCDSW\_3P3 [+VCCPDSW\_3P3] VCCPRIM\_1P8 [+VCCPRIM\_1P8] | 200 |  | us | VccDSW 3.3 stable (@95% of full value) to VccPrimary 1.8V starting to ramp (for DSx or nonDSx configurations) | PLT |  |
|  |
|  |
|  |
| **tPCH07** | DSW\_PWROK RSMRST# [PM\_RSMRST\_N] | 0 |  | ms | DSW\_PWROK high to RSMRST# high | PLT |  |
|  |
|  |
|  |
| **tPCH08** | SLP\_S3# [PM\_SLP\_S3\_N] PCH\_PWROK [PM\_PCH\_PWROK] | 1 |  | ms | SLP\_S3# de-assertion to PCH\_PWROK assertion | PLT |  |
|  |
|  |
|  |
| **tPCH32** | DSW\_PWROK SLP\_SUS# [PM\_SLP\_SUS\_N] | 95 |  | ms | DSW\_PWROK assertion to SLP\_SUS# de-assertion | PCH |  |
|  |
|  |
|  |
| **tCPU00** | VCCST [+VCCST\_CPU] VCCSTG [+VCCSTG\_CPU] VCCST\_PWRGD [VCCST\_PWRGD] | 2 |  | ms | VCCST, VCCSTG ramped and stable to VccST\_PWRGD assertion | PLT |  |
|  |
|  |
|  |
| **tCPU01** | DDR\_VDDQ [+VDD2\_MEM] VCCST\_PWRGD [VCCST\_PWRGD] | 1 |  | ms | VDDQ ramped and stable to VccST\_PWRGD assertion | PLT |  |
|  |
|  |
|  |
| **tPCH34** | VCCPRIM\_3P3 [+VCCPRIM\_3P3] V1.05A\_BYPASS [+VCC\_V1P05EXT\_1P05V] |  | 50 | ms | Time from start of ramp of the first prim rail after SLP\_SUS# deassertion to completion of primary and bypass rail ramp | PLT |  |
|  |
| VCCPRIM\_1P8 [+VCCPRIM\_1P8] V1.05A\_BYPASS [+VCC\_V1P05EXT\_1P05V] |  |
|  |

POWER DOWN:

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **SL. No** |  | **Rail Name** |  | **Net Name in SCH [Fill up by customer own design]** |  |
| 1 |  | PLTRST# | 1 | PLT\_RST\_N |  |
| 2 | PROCPWRGD | CPUPWRGD |  |
| 3 | 2 | SLP\_S3# | PM\_SLP\_S3\_N | USBAB\_VBUS=High |
| 4 | ALL\_SYS\_PWRGD |  | ALL\_SYS\_PWRGD |  |
| 5 | VCCST\_PWRGD | VCCST\_PWRGD  VCCST\_PWRGD must accurately reflect the state of VCCST and must not glitch when **VCCST**, **VCCSTG** or **VDDQ** power is applied. Additionally,  VCCST\_PWRGD must track to the state of PCH\_PWROK on the platform. When PCH\_PWROK de-asserts during S0 --> Sx transitions, then VCCST\_PWRGD must also de-assert. | VccST Power Good : When asserted, an indicator to the processor this rail is now supplied by the integrated FIVR in the PCH. |
| 6 | PCH\_PWROK | 3 | PM\_PCH\_PWROK |  |
| 7 |  | SYS\_PWROK | SYS\_PWROK |  |
| 8 | VCCIN | +VCCIN |  |
| 9 | 4 | VTT | +V\_VDD2\_VTT |  |
| 10 | VCCSTG |  | +VCCSTG\_CPU |  |
| 11 | SLP\_S4# | PM\_SLP\_S4\_N | In Tensor I22:  If SLP\_S4#=0 -> USBAB\_VBUS=0 |
| 12 | **DDR\_VDDQ (DDR4)** | 5 | **+VDD2\_MEM** |  |
| 13 |  | VCCST | +VCCST\_CPU |  |
| 14 | SLP\_S5# | PM\_SLP\_S5\_N |  |
| 15 | 6 | **DDR\_VPP (DDR4)** | **+V1.8U\_2.5U\_MEM** |  |
| 16 | SLP\_SUS# |  | PM\_SLP\_SUS\_N |  |
| 17 | DSW\_PWROK | 7 | DSW\_PWROK |  |
| 18 |  | RSMRST# | PM\_RSMRST\_N |  |
| 19 | SLP\_S0# | PM\_SLP\_S0\_N | S0 Sleep Control. When PCH is idle and processor is in C10 state, this  Pin will assert indicate VR controller can go into a light load mode. This signal can also be connected to EC for other power management related optimizations. |
| 20 | 8 | CPU\_C10\_GATE# | CPU\_C10\_GATE\_N |  |
| 21 | VCCDSW\_3P3 |  | +VCCPDSW\_3P3 |  |
| 22 | V5.0A | +V5A |  |
| 23 | VCCPRIM\_3P3 | 9 | +VCCPRIM\_3P3 |  |
| 24 |  | VCCPRIM\_1P8 | +VCCPRIM\_1P8 |  |
| 25 | VCC1.05\_OUT\_PCH | +VCC1P05\_OUT\_PCH |  |
| 26 | 10 | VCCIN\_AUX | +VCCIN\_AUX |  |
| 27 | VNN\_BYPASS |  | +VCC\_VNNEXT\_1P05V |  |
| 28 | V1.05A\_BYPASS | +VCC\_V1P05EXT\_1P05V |  |
| 29 | PWRBTN# | 11 | PM\_PWRBTN\_N |  |
| 30 |  | VCCRTC | +VCCPRTC\_3P3 |  |
| 31 | RTCRST# | RTC\_RST\_N |  |
| 32 | SRTCRST# | SRTC\_RST\_N |  |

SLP\_A#:

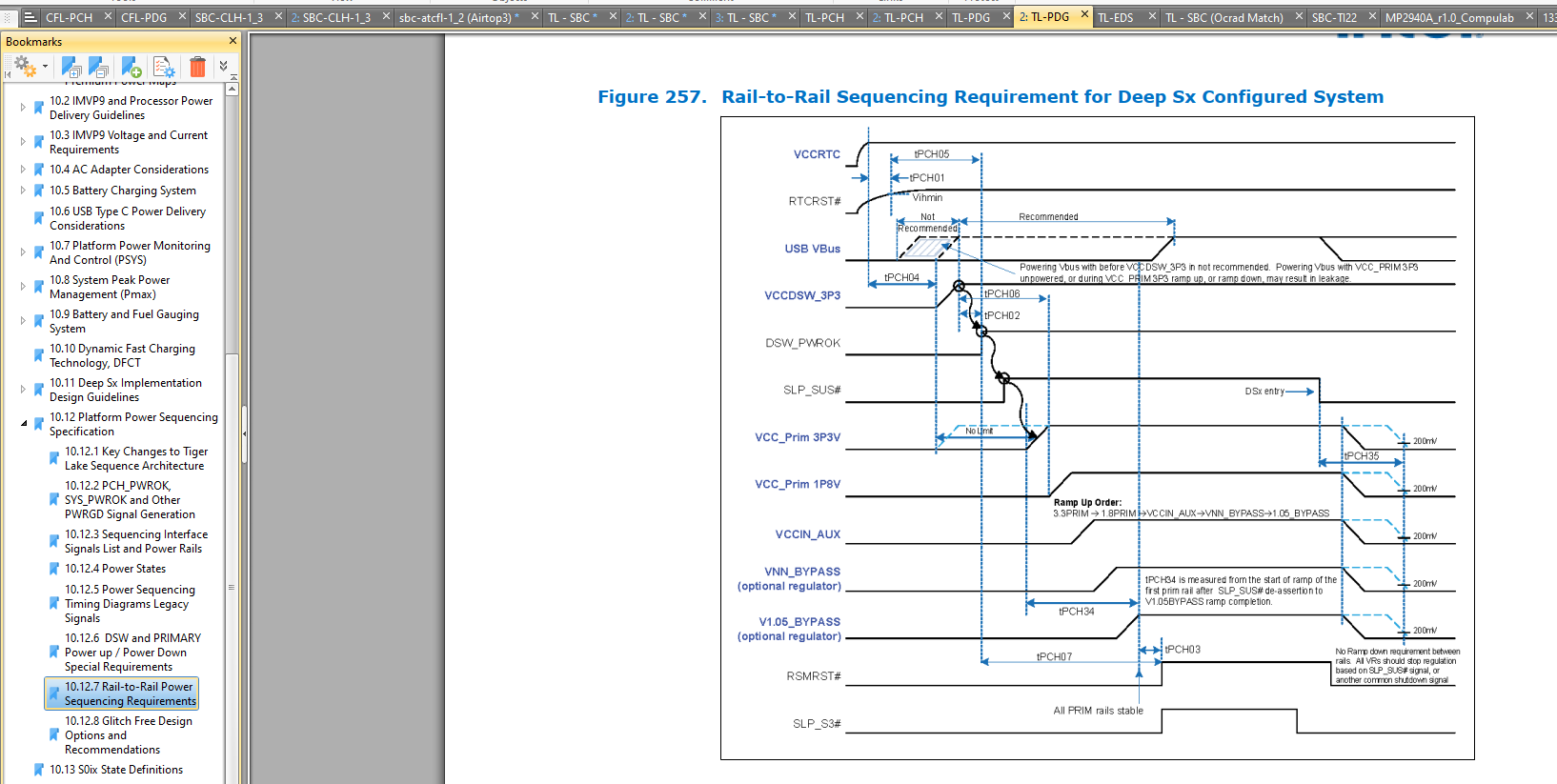


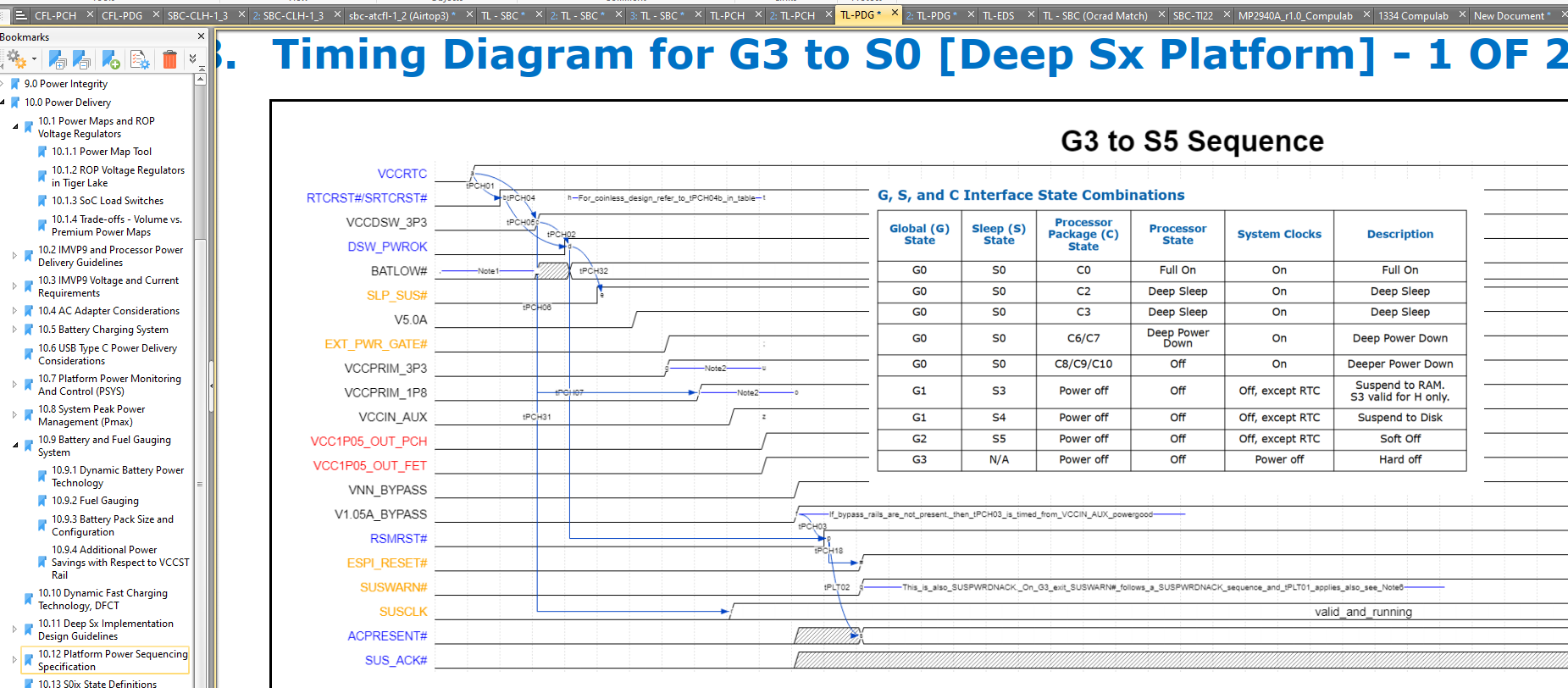


Power Down:

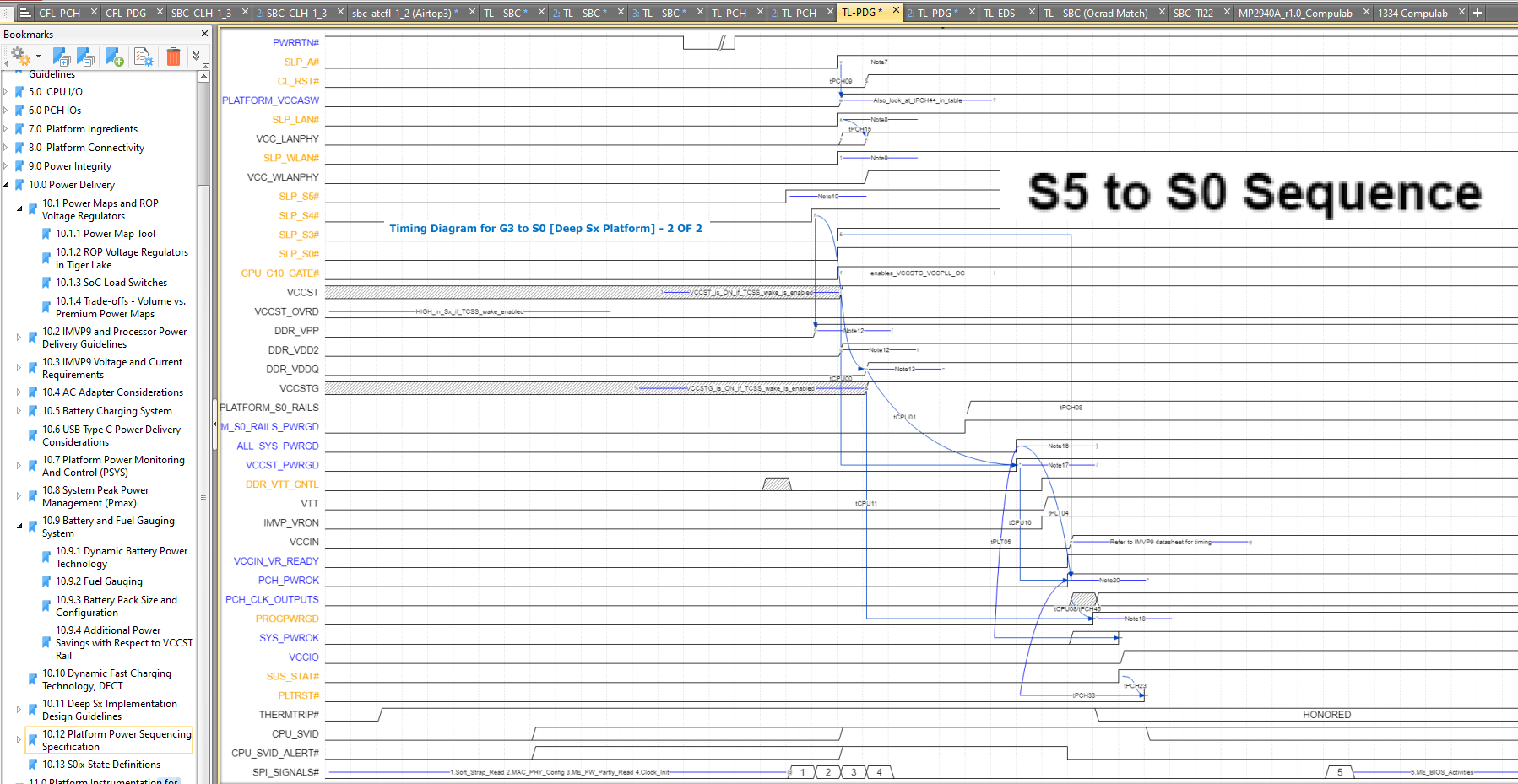
|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **Label** | **Signal Name** | **Min** | **Max** | **Unit** | **Description** | **Controlled by** |
| **tPCH24** | PLTRST# [PLTRST\_N] PROCPWRGD [CPUPWRGD] | 30 |  | us | PLTRST# assertion to PROCPWRGD de-assertion | PCH |
|
|
|
| **tPCH27** | SLP\_S4# [PM\_SLP\_S4\_N] SLP\_S5# [PM\_SLP\_S5\_N] | 30 |  | us | SLP\_S4# assertion to SLP\_S5# assertion | PCH |
|
|
|
| **tPCH28** | SLP\_S3# [PM\_SLP\_S3\_N] SLP\_S4# [PM\_SLP\_S4\_N] | 30 |  | us | SLP\_S3# assertion to SLP\_S4# assertion | PCH |
|
|
|
| **tCPU22** | VCCST\_PWRGD [VCCST\_PWRGD] DDR\_VDDQ [+VDD2\_MEM] | 1 |  | us | VCCST\_PWRGD deassertion to either VDDQ, VCCST, VCCSTG below specification for normal S0 to Sx transitions. Recommend VCCST\_PWRGD goes low with SLP\_S3# | PLT |
|
| VCCST\_PWRGD [VCCST\_PWRGD] VCCST [+VCCST\_CPU] |
|
| VCCST\_PWRGD [VCCST\_PWRGD] VCCSTG [+VCCSTG\_CPU] |
|
| **tPCH29** | SLP\_S3# [PM\_SLP\_S3\_N] PCH\_PWROK [PM\_PCH\_PWROK] | 0 |  | ms | SLP\_S3# assertion to PCH\_PWROK deassertion | PCH |
|
|
|

Power Sequence

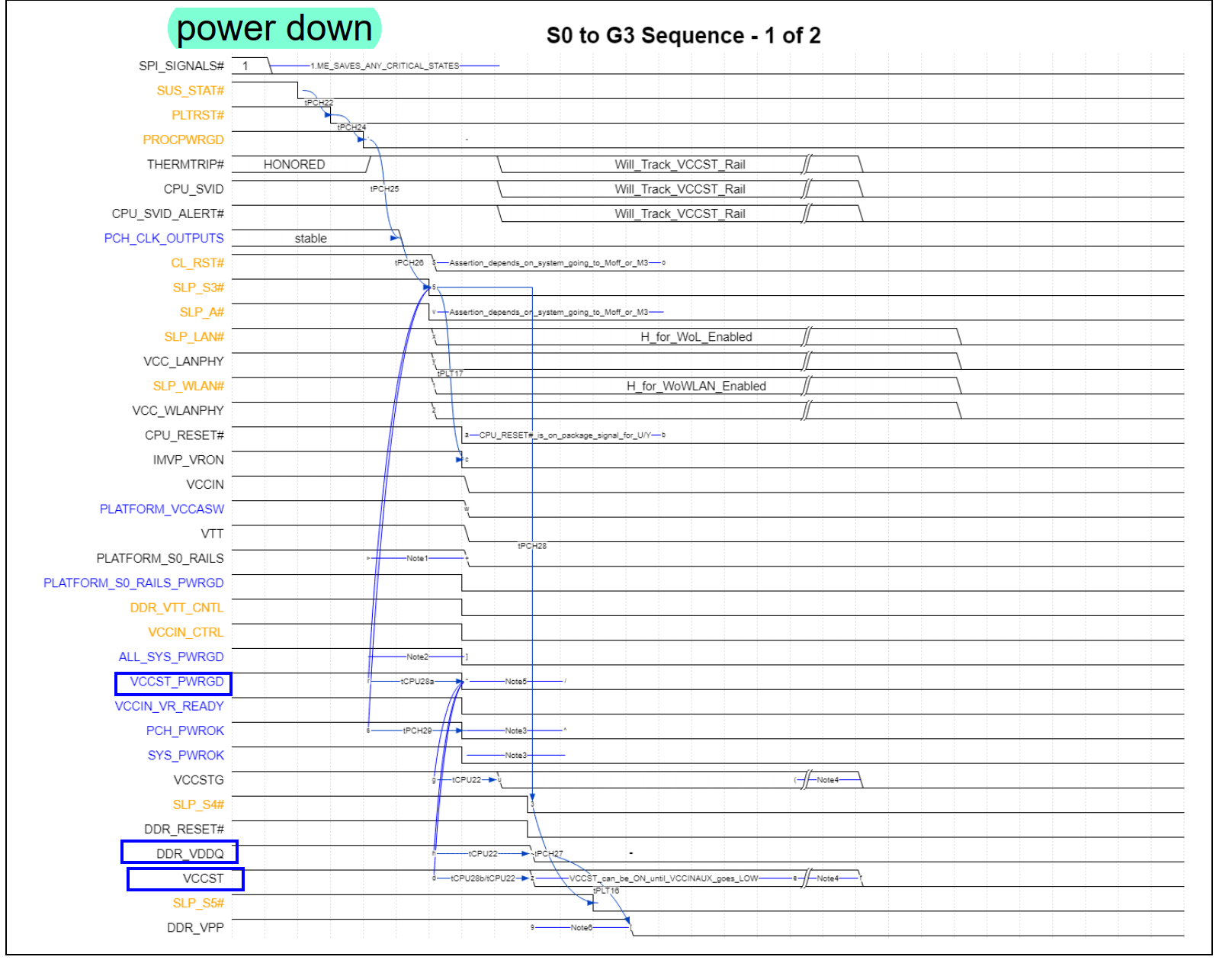




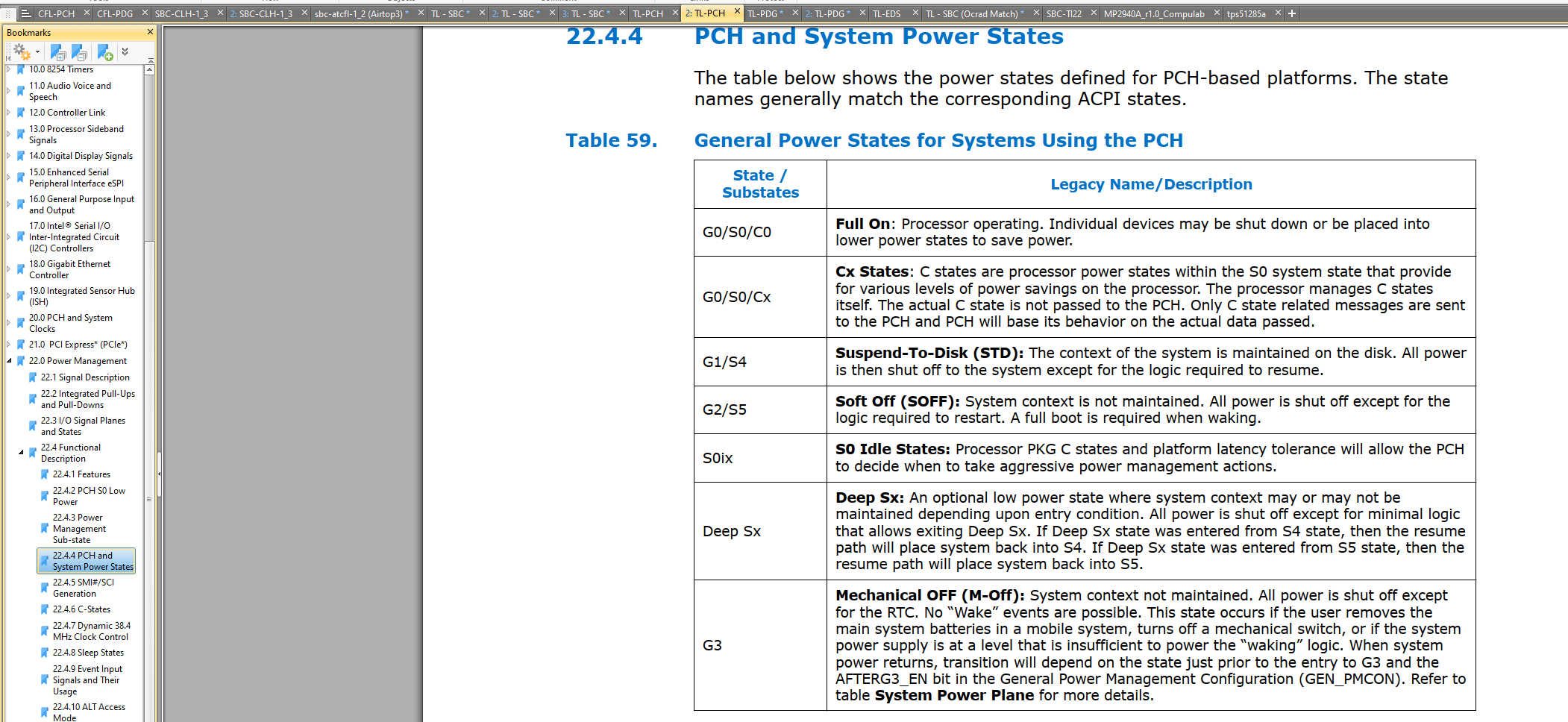
Power Up:



Power down:

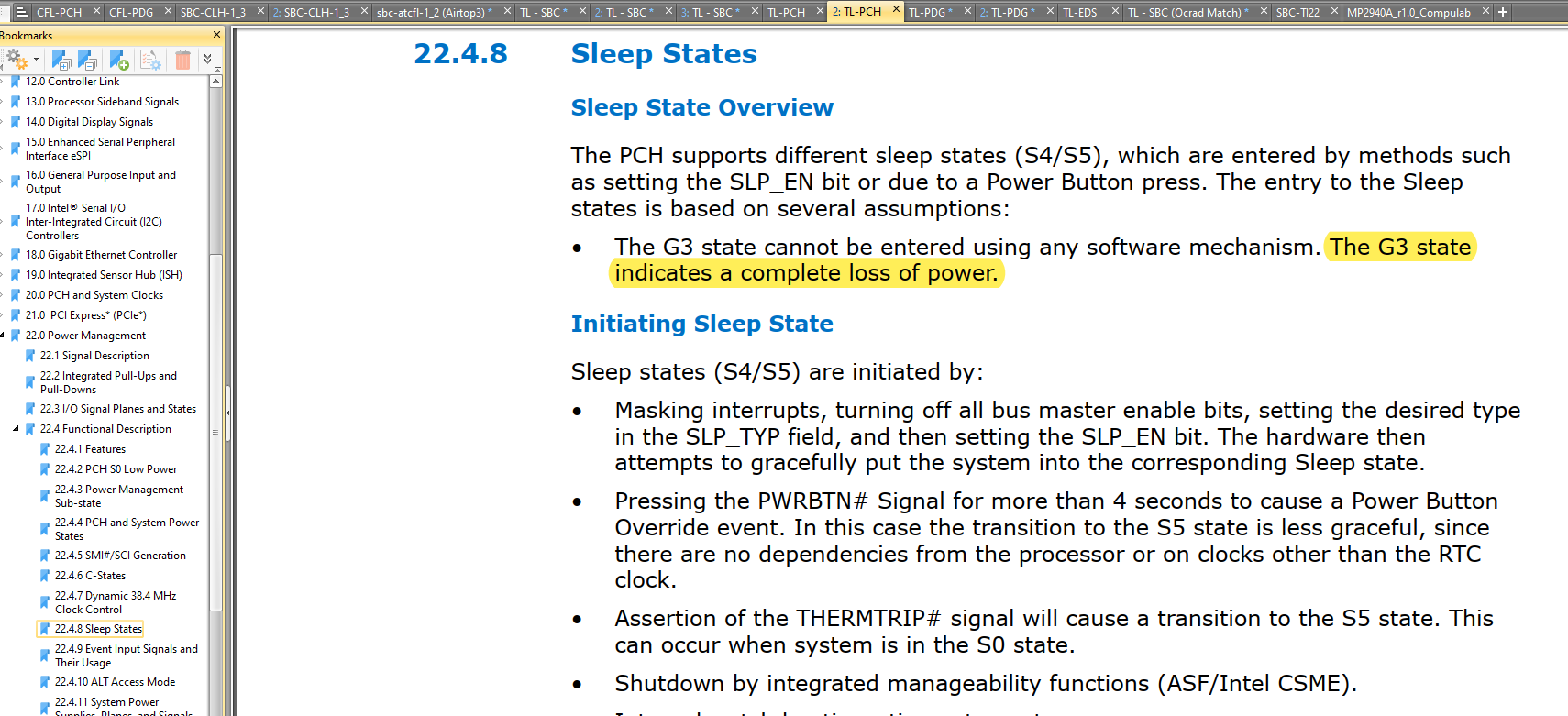


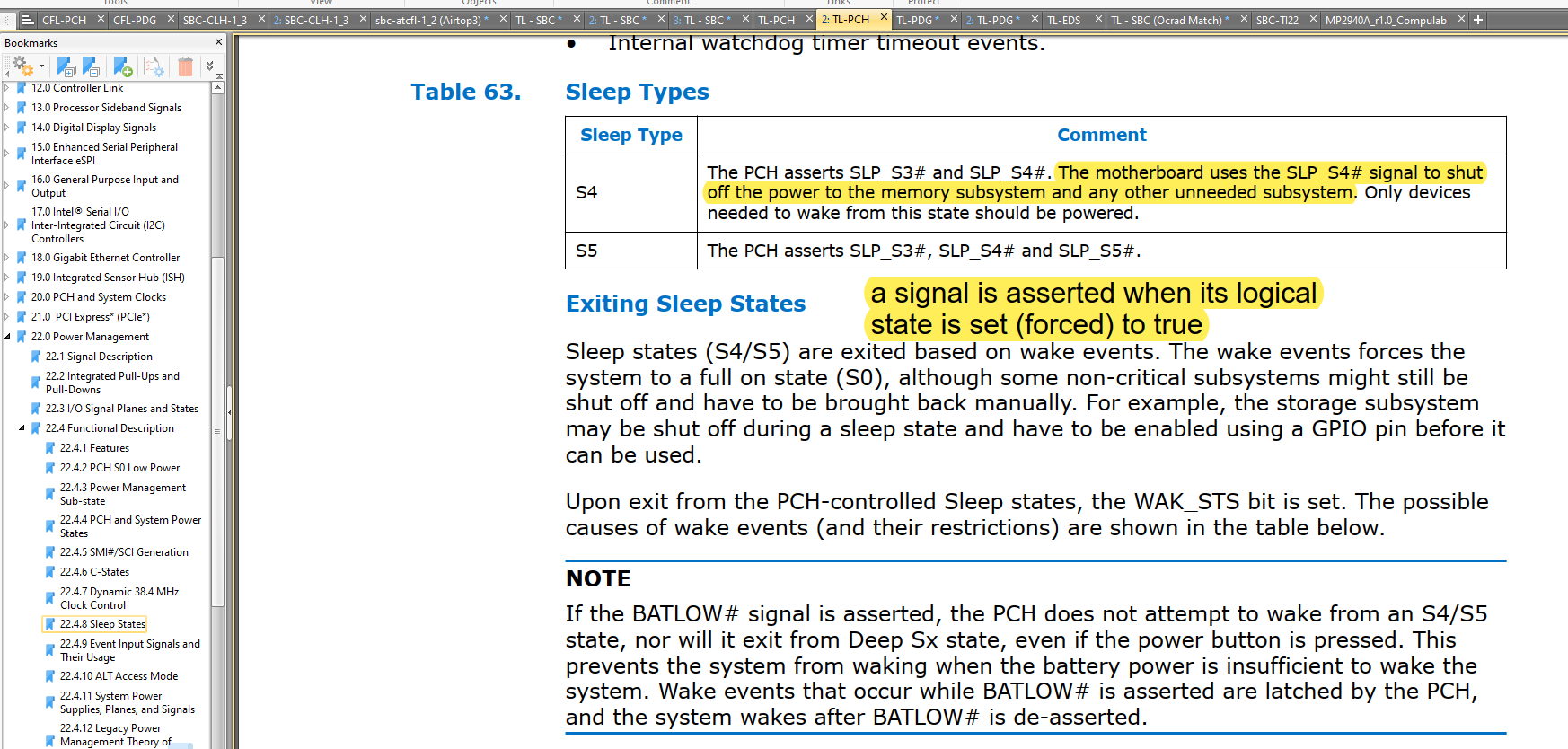
**PCH:**

****

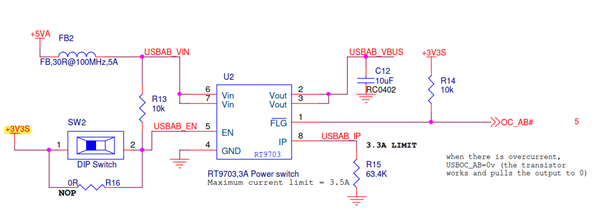
|  |  |
| --- | --- |
| **State /**  **Substates** | **Legacy Name/Description** |
| **G0/S0/C0** | **Full On: Processor operating. Individual devices may be shut down or be placed into lower power states to save power.** |
| **G0/S0/Cx** | **Cx States: C states are processor power states within the S0 system state that provide for various levels of power savings on the processor. The processor manages C states itself. The actual C state is not passed to the PCH. Only C state related messages are sent to the PCH and PCH will base its behavior on the actual data passed.** |
| **G1/S4** | **Suspend-To-Disk (STD): The context of the system is maintained on the disk. All power is then shut off to the system except for the logic required to resume.** |
| **G2/S5** | **Soft Off (SOFF): System context is not maintained. All power is shut off except for the logic required to restart. A full boot is required when waking.** |
| **S0ix** | **S0 Idle States: Processor PKG C states and platform latency tolerance will allow the PCH to decide when to take aggressive power management actions.** |
| **Deep Sx** | **Deep Sx: An optional low power state where system context may or may not be maintained depending upon entry condition. All power is shut off except for minimal logic that allows exiting Deep Sx. If Deep Sx state was entered from S4 state, then the resume path will place system back into S4. If Deep Sx state was entered from S5 state, then the resume path will place system back into S5.** |
| **G3** | **Mechanical OFF (M-Off): System context not maintained. All power is shut off except for the RTC. No “Wake” events are possible. This state occurs if the user removes the main system batteries in a mobile system, turns off a mechanical switch, or if the system power supply is at a level that is insufficient to power the “waking” logic. When system power returns, transition will depend on the state just prior to the entry to G3 and the AFTERG3\_EN bit in the General Power Management Configuration (GEN\_PMCON). Refer to table System Power Plane for more details.** |

Sleep States

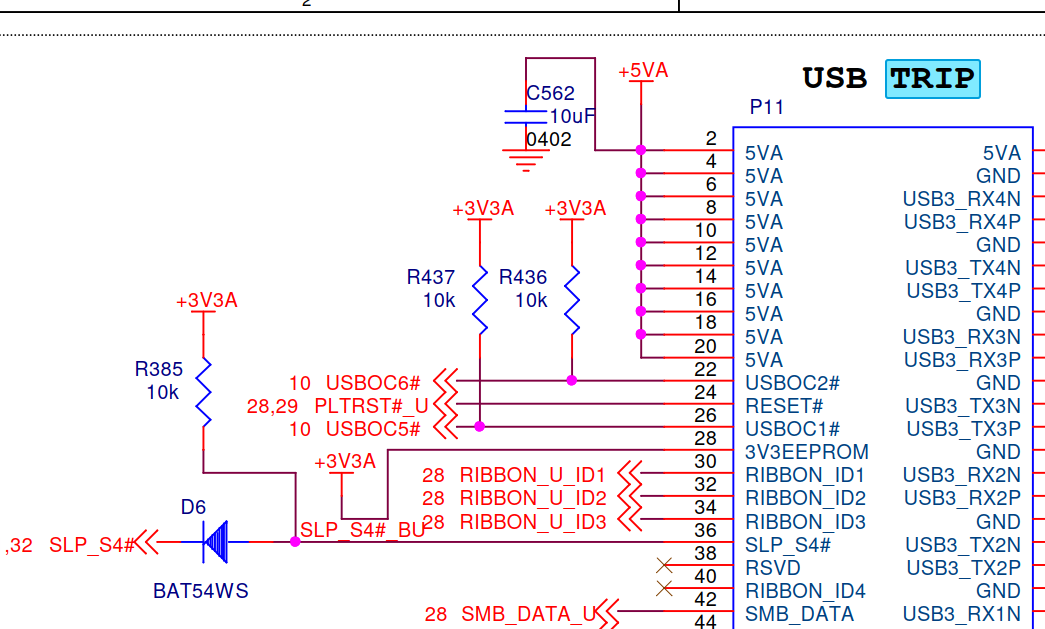




USB:



Every USB port must always have VBUS when the system is on S3.  
Having that, the wanted status is to turn the VBUS of on S4 and S5, and addition of a switch to change it is a good feature.



When SLP\_S4# = 0 (from the CPU) then SLP\_S4#=1 inside the TEL.

And if we turn the switch ON, that means SLP\_S4#=1 will enable VBUS even when the CPU is in S4 and S5.